CLAIMS

1. (Currently amended) A process for fabricating a semiconductor device comprising:

providing a semiconductor substrate having formed thereon a semiconductor device;

depositing over the semiconductor device a spacer layer, the spacer layer having a first hydrogen content; and

applying a treatment to reduce the first hydrogen content to a second hydrogen content,

wherein the treatment comprises one or more of RTO oxidation of at least a portion of the spacer layer in an oxidizing atmosphere, ISSG oxidation of at least a portion of the spacer layer, free radical oxidation of at least a portion of the spacer layer, decoupled plasma oxidation of at least a portion of the spacer layer, and steam oxidation of at least a portion of the spacer layer at a temperature in the range from about 400°C to about 1100°C.

2. (Canceled)

3. (Original) The process of claim 1, wherein the first hydrogen content is in a range from greater than about 2 atomic percent to about 30 atomic percent.

4. (Original) The process of claim 1, wherein the second hydrogen content is less than about two atomic percent.

5. (Original) The process of claim 4, wherein the second hydrogen is in the range from about 0.1 atomic percent to about 0.5 atomic percent.

6. (Original) The process of claim 4, wherein the second hydrogen content is substantially zero or not detectable by FTIR.

7. (Original) The process of claim 1, wherein hydrogen substantially does not migrate into the semiconductor device from the spacer layer during subsequent processing or in use.

8. (Original) The process of claim 1, wherein the treatment is applied to the spacer layer, prior to etching to form a spacer for the semiconductor device.

9. (Original) The process of claim 1, wherein the process further comprises a step of etching to form a spacer for the semiconductor device, and the treatment is applied to the spacer subsequent to the etching step.

10. (Original) A process for fabricating a charge trapping dielectric flash memory device comprising:

providing a semiconductor substrate having formed thereon a gate stack comprising a charge trapping dielectric charge storage layer and a control gate electrode overlying the charge trapping dielectric charge storage layer;

depositing over the gate stack a spacer layer, the spacer layer having a first hydrogen content; and

applying a treatment to reduce the first hydrogen content of at least a portion of the spacer layer to a second hydrogen content.

11. (Original) The process of claim 10, wherein the treatment comprises one or more of RTO oxidation of at least a portion of the spacer layer in an oxidizing atmosphere, ISSG oxidation of at least a portion of the spacer layer , free radical oxidation of at least a portion of the spacer layer, decoupled plasma oxidation of at

least a portion of the spacer layer, and steam oxidation of at least a portion of the spacer layer at a temperature in the range from about 400°C to about 1100°C.

12. (Original) The process of claim 10, wherein the first hydrogen content is in a range from greater than about 2 atomic percent to about 30 atomic percent.

13. (Original) The process of claim 10, wherein the second hydrogen content is less than about two atomic percent.

14. (Original) The process of claim 13, wherein the second hydrogen is in the range from about 0.1 atomic percent to about 0.5 atomic percent.

15. (Original) The process of claim 13, wherein the second hydrogen content is substantially zero or not detectable by FTIR.

16. (Original) The process of claim 10, wherein hydrogen substantially does not migrate into the gate stack from the spacer layer during subsequent processing or in use.

17. (Original) The process of claim 10, wherein the treatment is applied to the spacer layer, prior to an etching step for forming a gate stack spacer.

18. (Original) The process of claim 1, wherein the treatment is applied to the gate stack spacer subsequent to an etching step for forming a gate stack spacer.

19. (Original) A charge trapping dielectric flash memory device comprising:

a semiconductor substrate having formed thereon a gate stack comprising a charge trapping dielectric charge storage layer and a control gate electrode overlying the charge trapping dielectric charge storage layer; and

a gate stack spacer adjacent sides of the gate stack,

wherein the gate stack spacer comprises a hydrogen content less than about two atomic percent.

20. (Original) The device of claim 19, wherein the hydrogen content is in the range from about 0.1 atomic percent to about 0.5 atomic percent.

21. (New) The device of claim 19, wherein the hydrogen content is substantially zero or not detectable by FTIR.